ABSTRACT

A method and system for reducing power consumption in a processor core. A state machine used to coordinate a frequency from a clock signal generator with a voltage from a voltage regulator which is sufficient to allow operation of the processor at that frequency. Bot the clock signal generator and the voltage regulator must be able to generate at least two frequencies or voltages, respectively. A level of processor need is tracked and the lowest frequency/ voltage pair that will allow the processor core to satisfy the need is selected. The level of processor need is monitored either periodically or continually such that a new frequency / voltage pair can be dynamically selected as the application mix change